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1 36159/JWE/B600

LOW JITTER HIGH PHASE RESOLUTION PLL-BASED
TIMING RECOVERY SYSTEM

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ABSTRACT OF THE DISCLOSURE

10 A low jitter, high phase resolution phase lock loop
incorporating a ring oscillator-type VCO is designed and
constructed to operate at a characteristic frequency M times
higher than a required output clock frequency. Multi-phase
output signals are taken from the VCO and selected through a Gray
code MUX, prior to being divided down to the output clock
frequency by a divide-by-M frequency divider circuit. Operating
15 the VCO at frequencies in excess of the output clock frequency,
allows jitter to be averaged across a timing cycle M and further
allows a reduction in the number of output phase taps, by a scale
factor M, without reducing the phase resolution or granularity
of the output signal.

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